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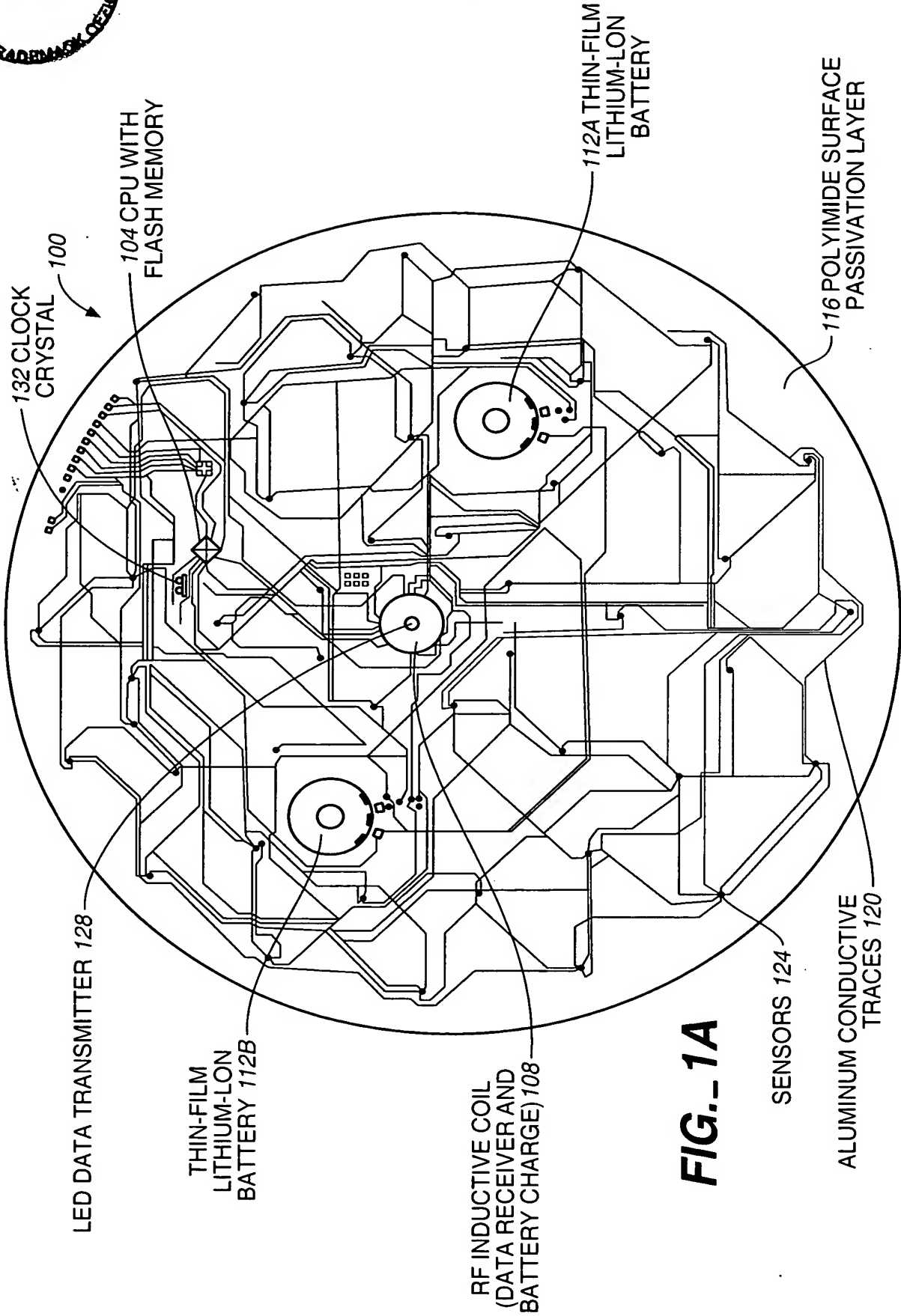


FIG. 1A

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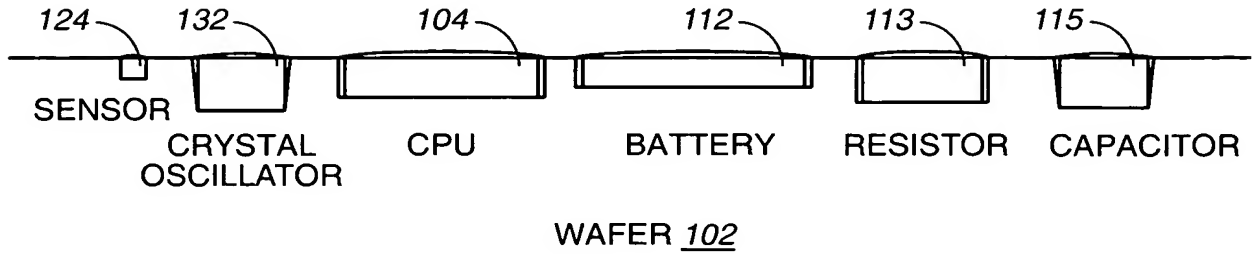


FIG. 1B

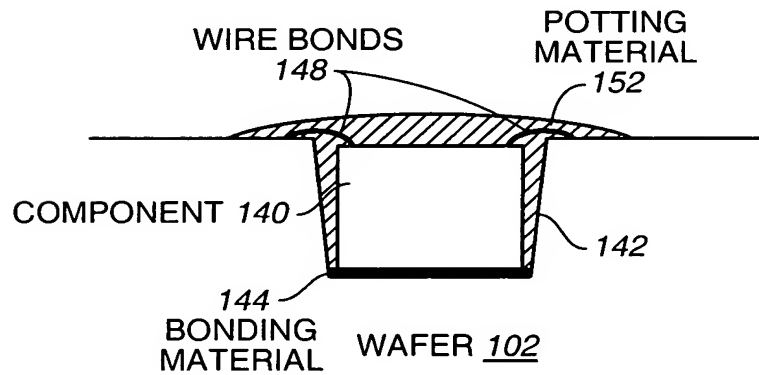


FIG. 1C

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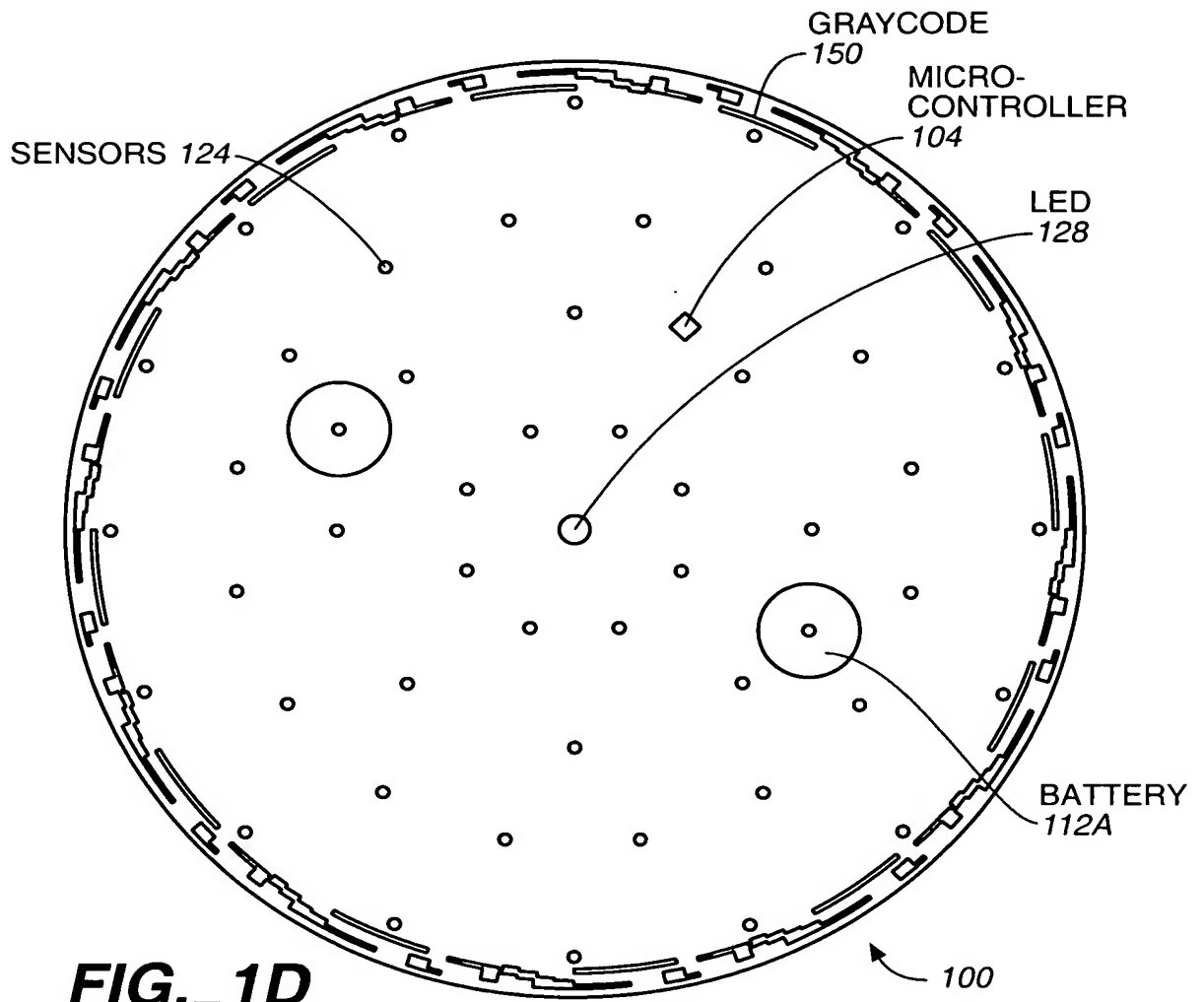


FIG. 1D

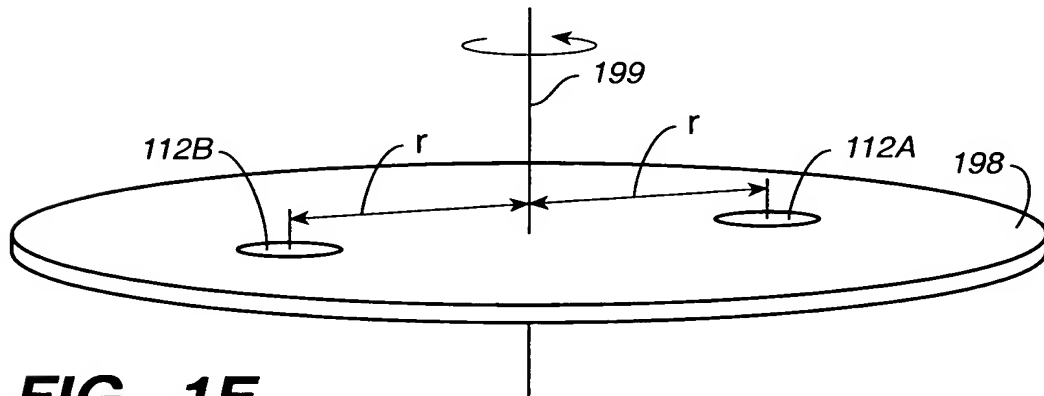
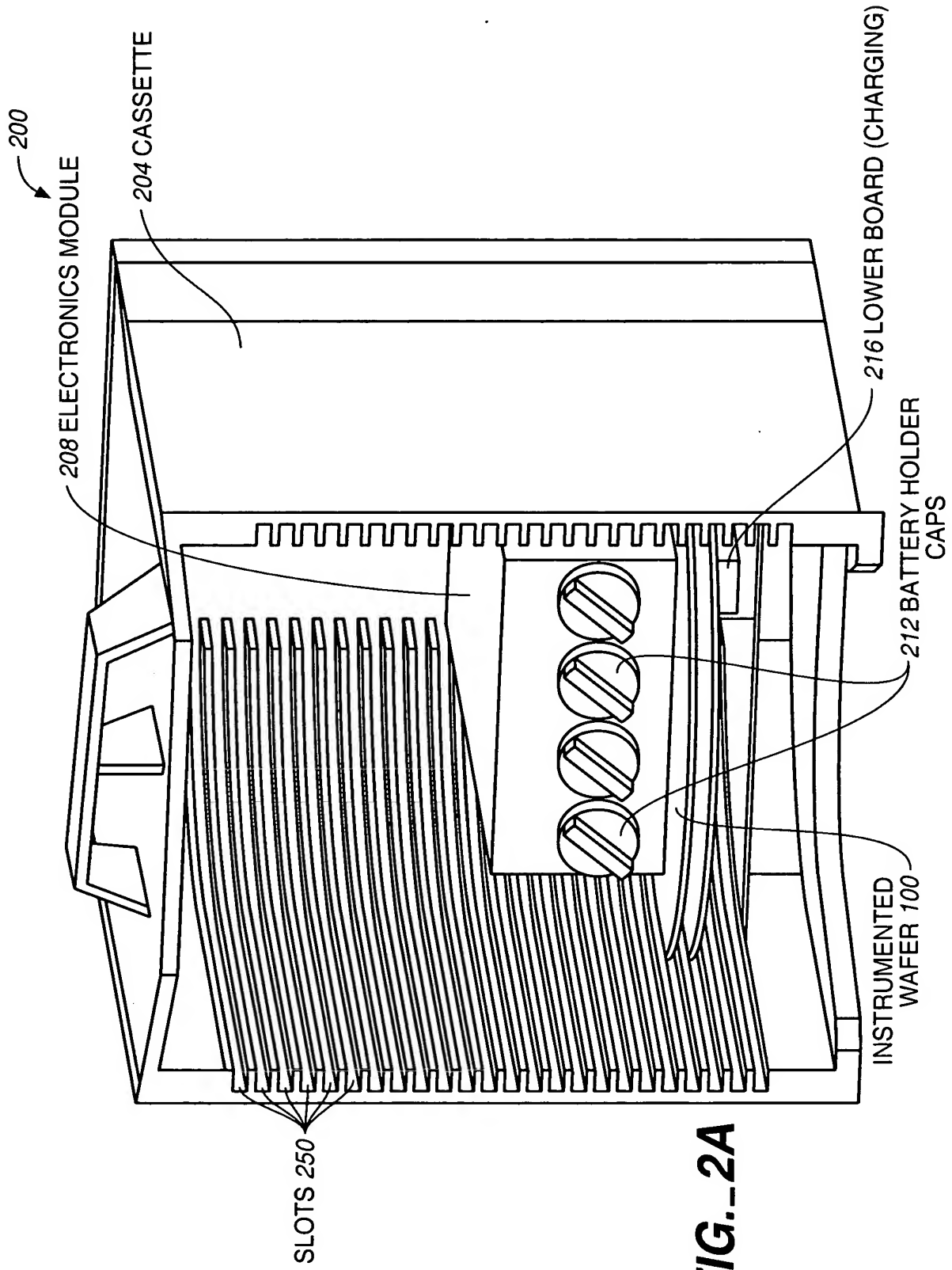


FIG. 1E



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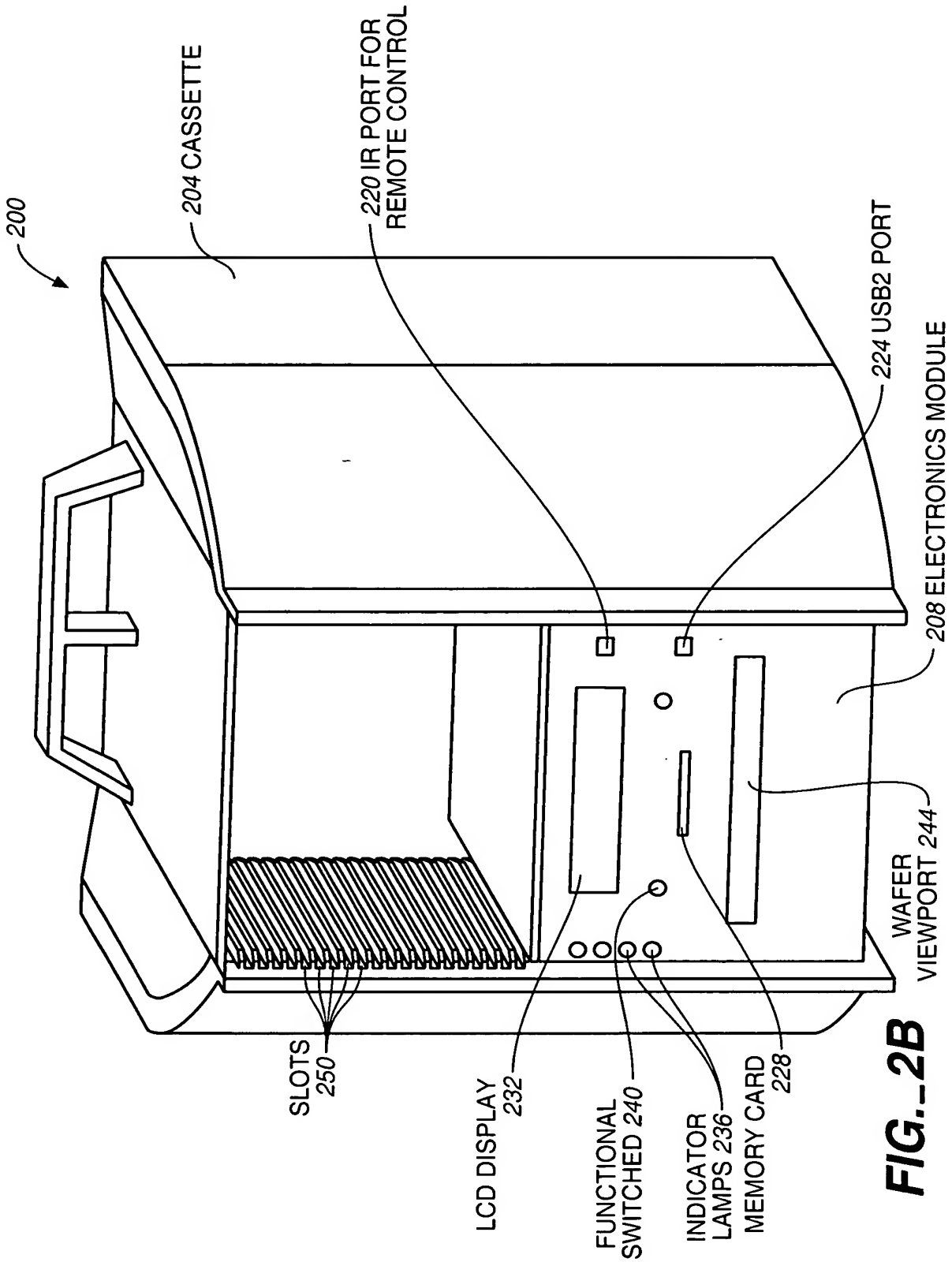


FIG. 2B

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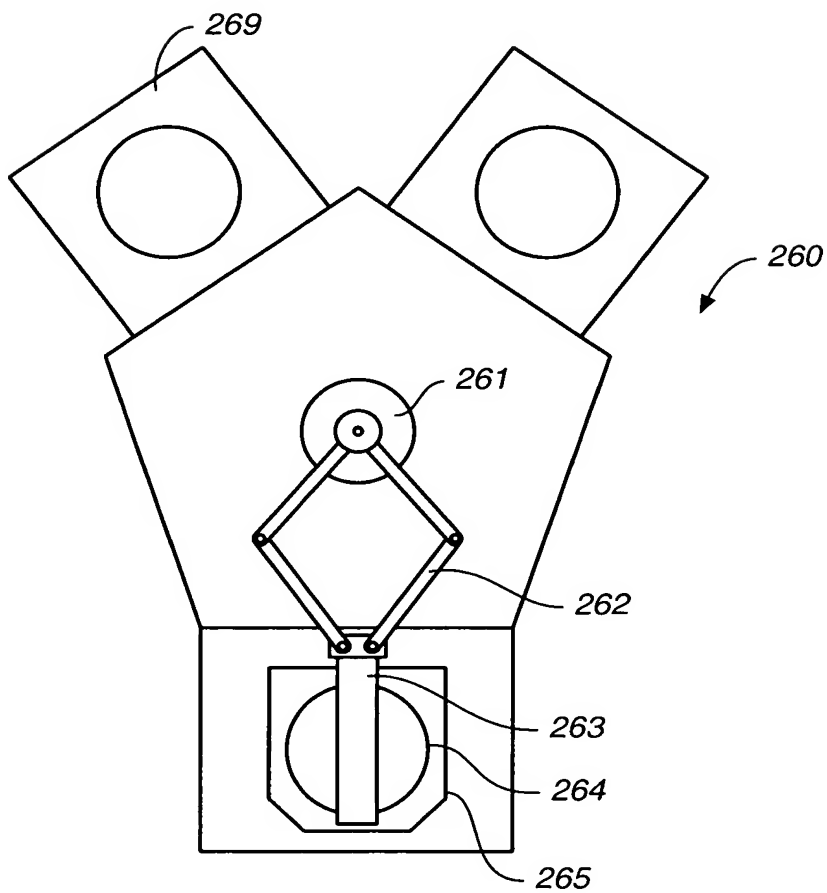


FIG. 2C

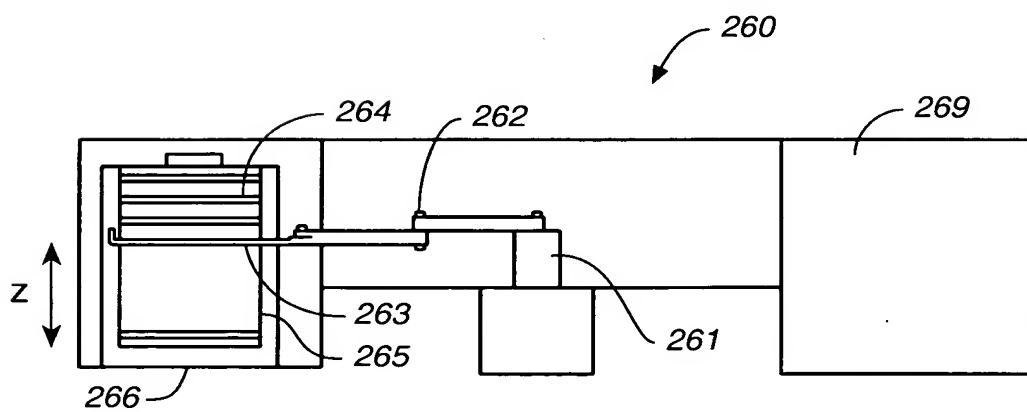


FIG. 2D

A cross-sectional view of a semiconductor device. The structure is built on a **WAFER 102** (indicated by a wavy line at the bottom). A **METAL VIA 312C** is formed in the wafer. Above the wafer is a layer of **SILICON OXIDE 304** (stippled pattern). On top of the silicon oxide is a layer of **SILICON NITRIDE 308** (fine horizontal lines). Above the silicon nitride is a layer of **INTER-LEVEL DIELECTRIC 310** (diagonal lines). A **BOND PAD OPENING (NOT TO SCALE) 320** is formed in the inter-level dielectric. The opening is filled with **POLYIMIDE 316** (diagonal lines). The opening is bounded by **312A** (left wall) and **312B** (right wall), which are the silicon nitride layer. The bottom of the opening is defined by the **312C** metal via.

+

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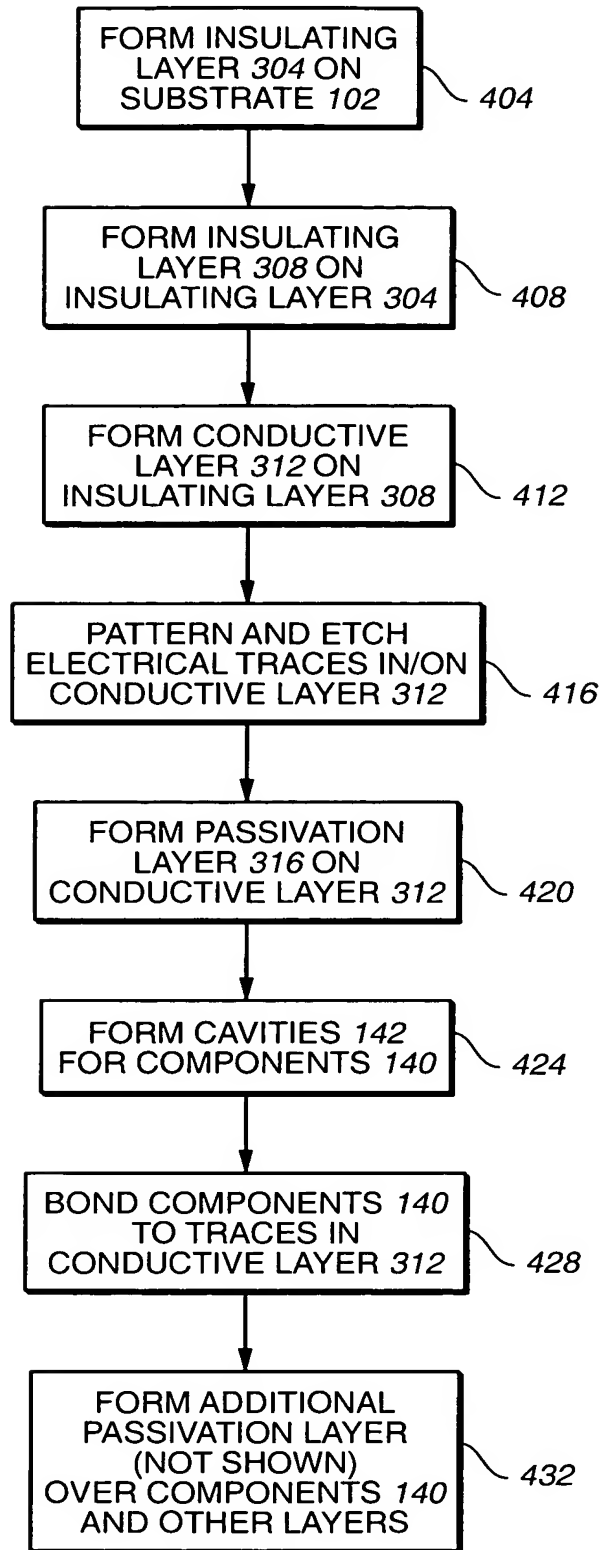


FIG._4A

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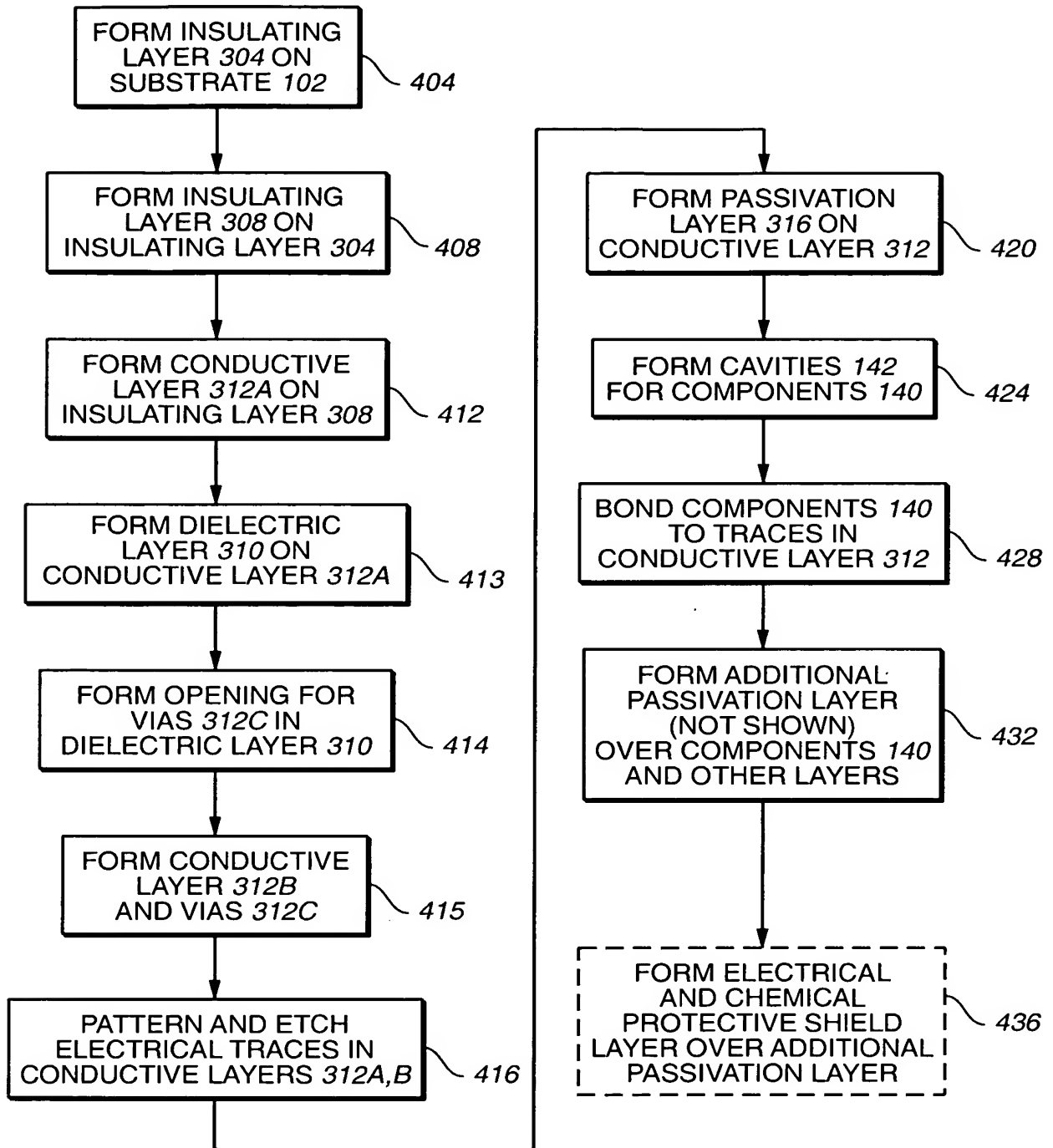


FIG. 4B

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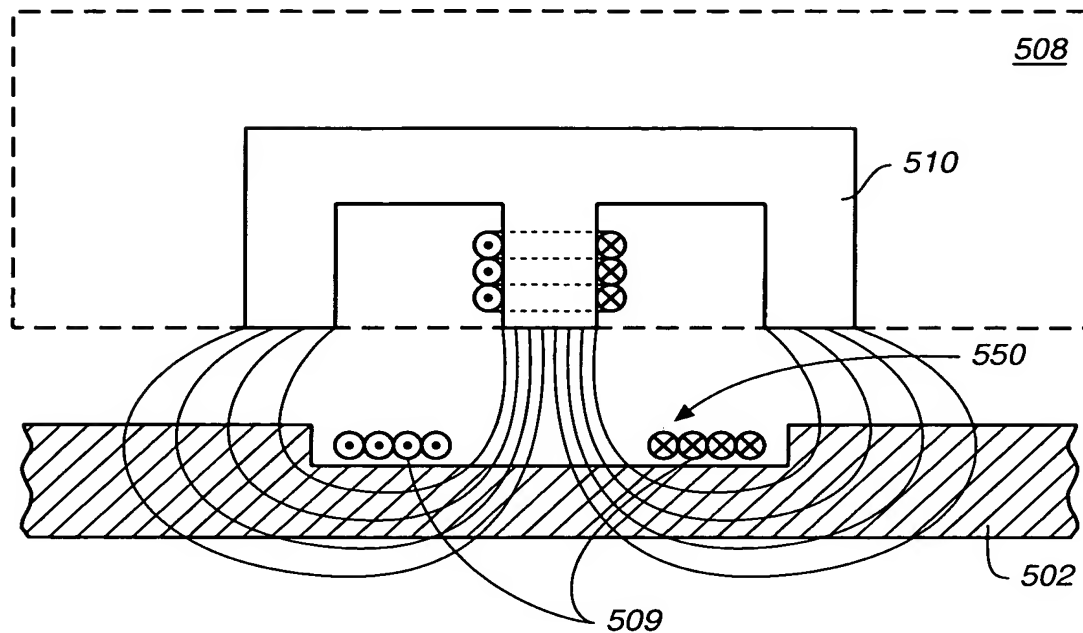


FIG._5A

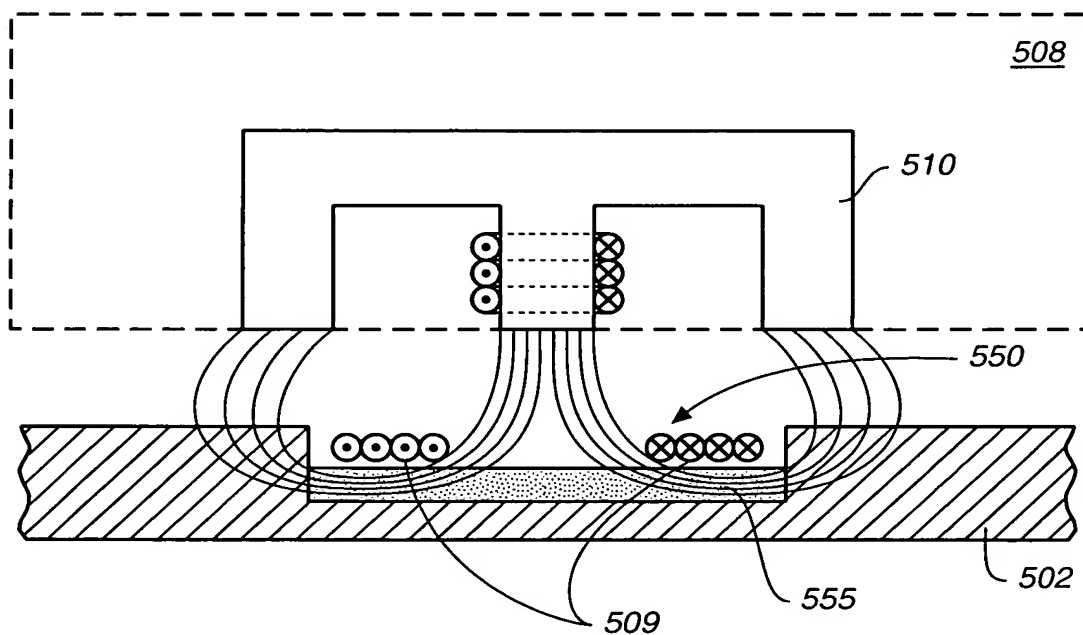


FIG._5B

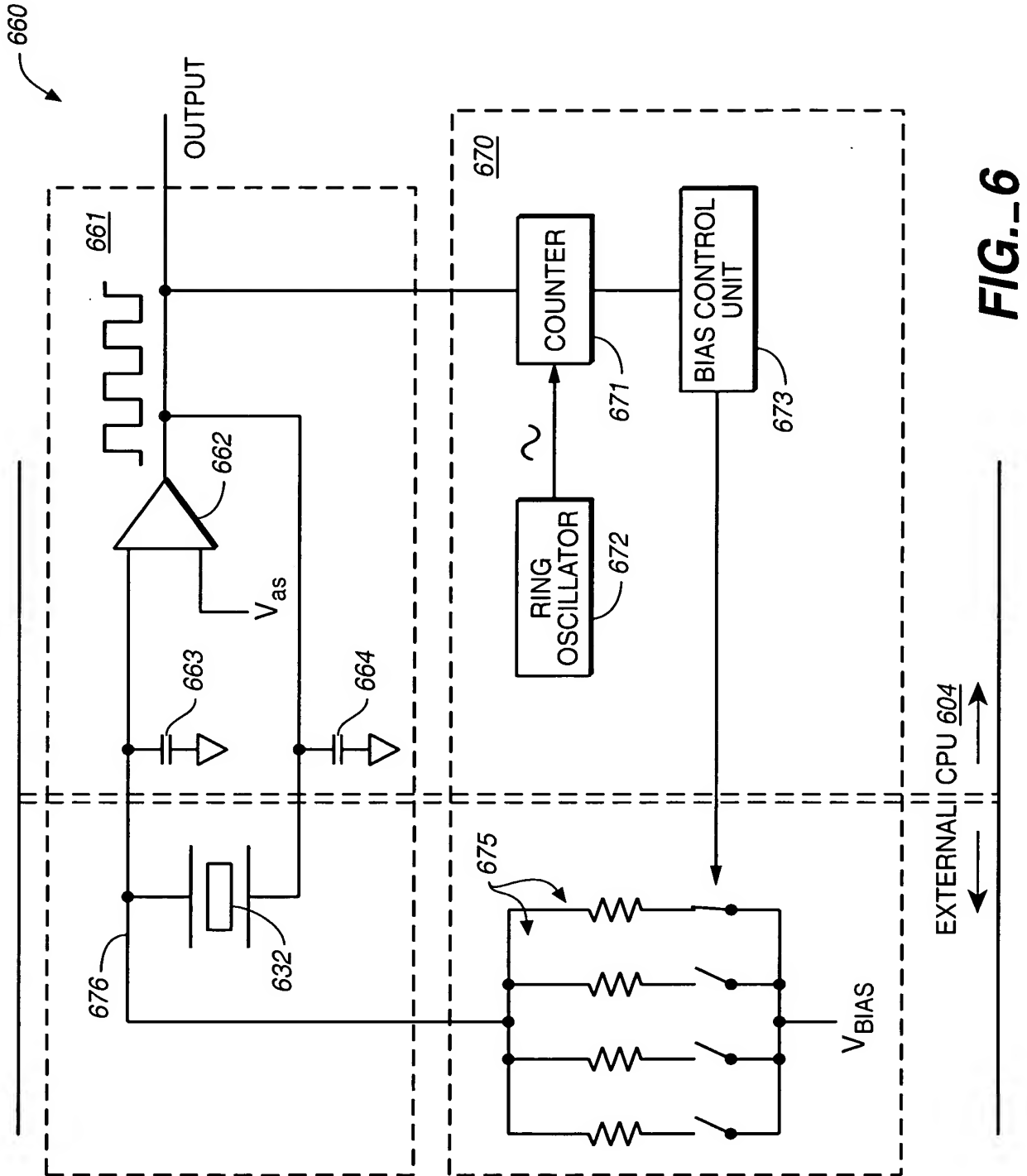


FIG. 6

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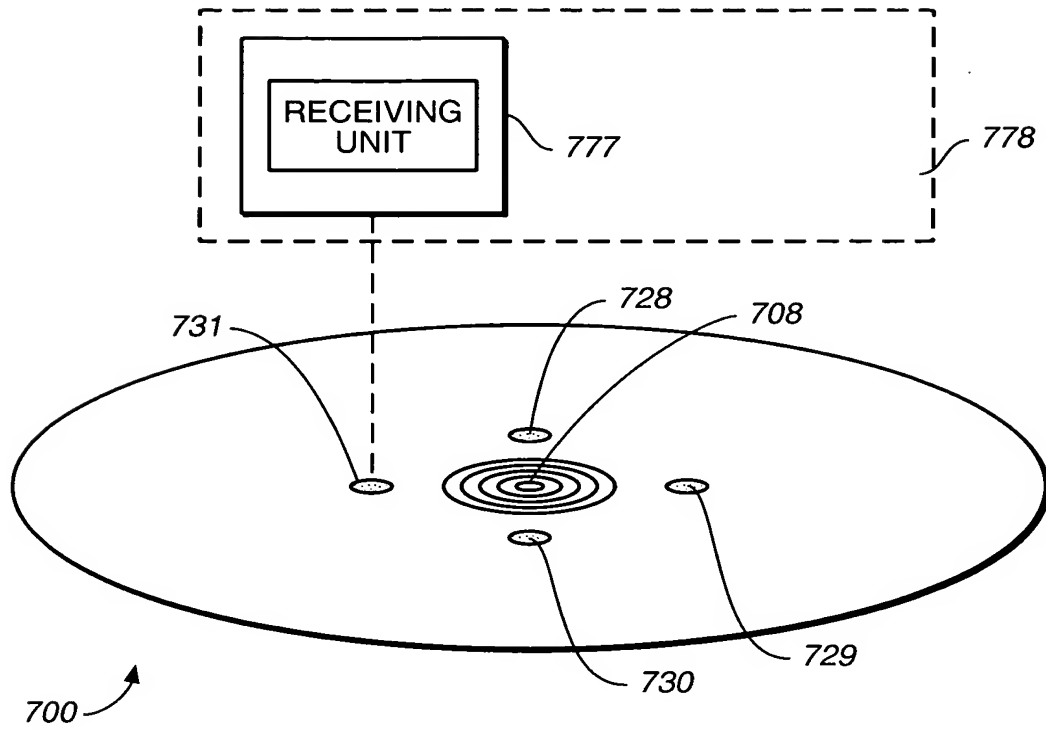


FIG. 7

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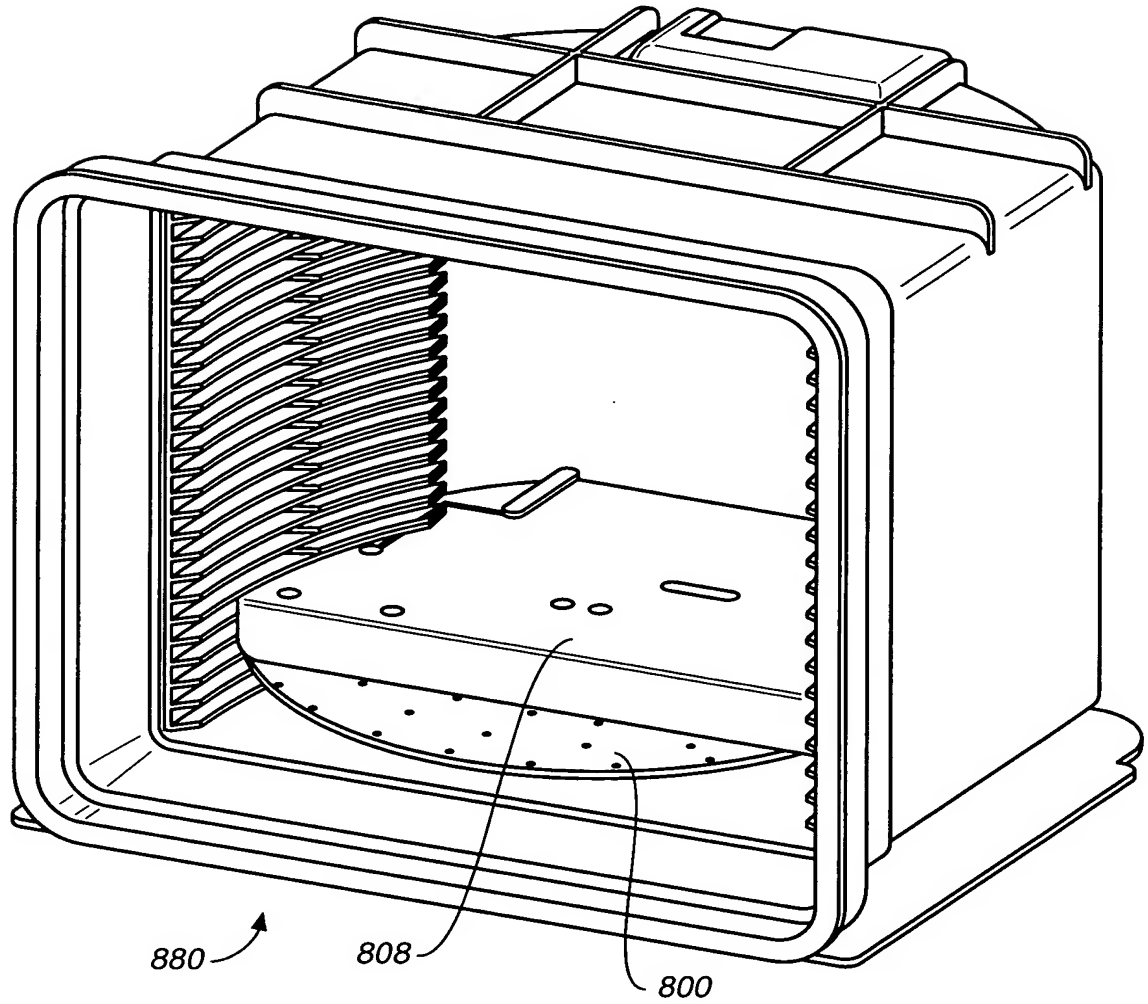


FIG. 8A

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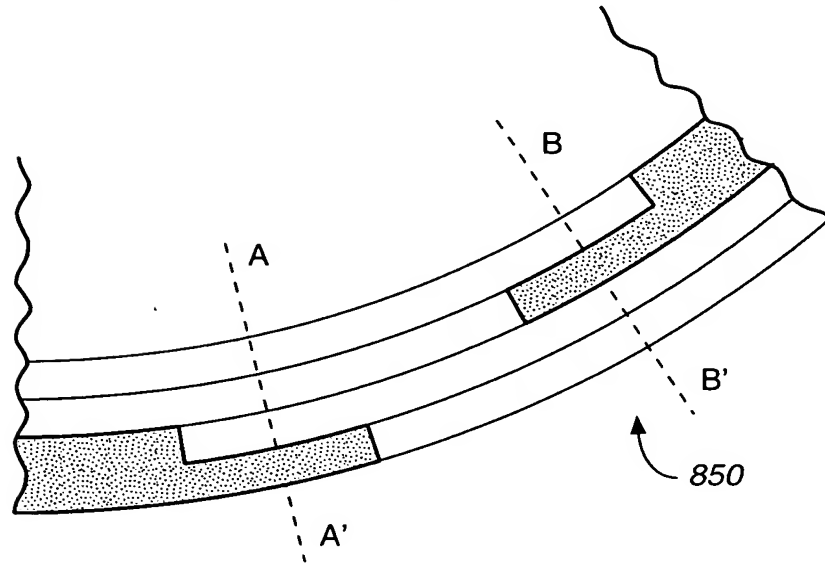


FIG._8B

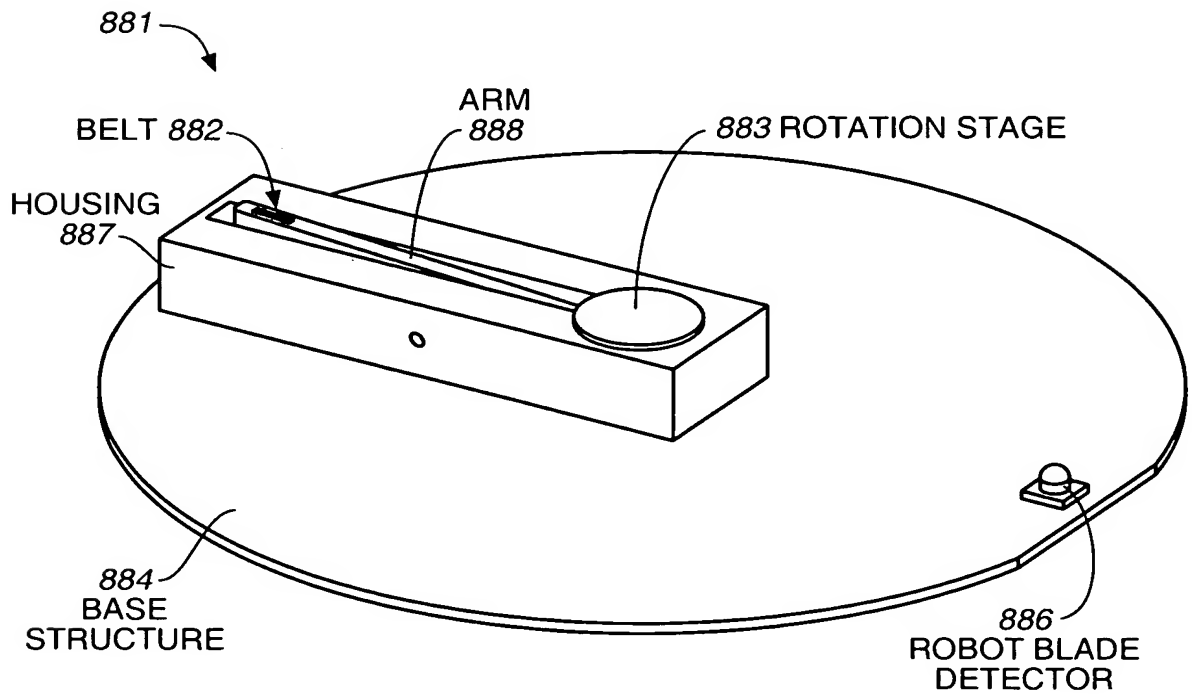
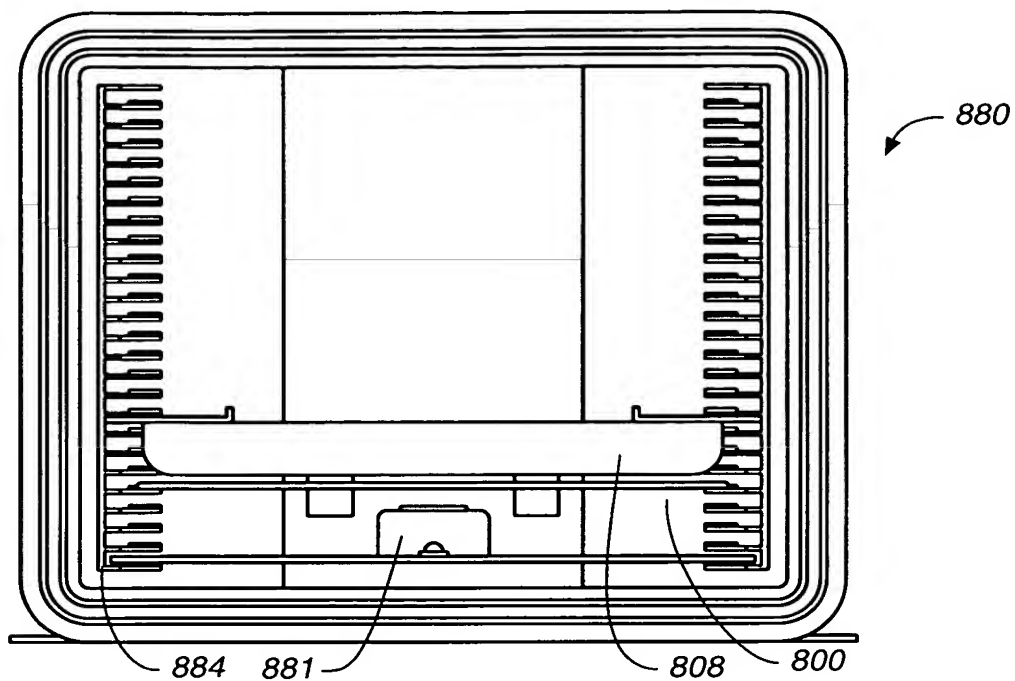


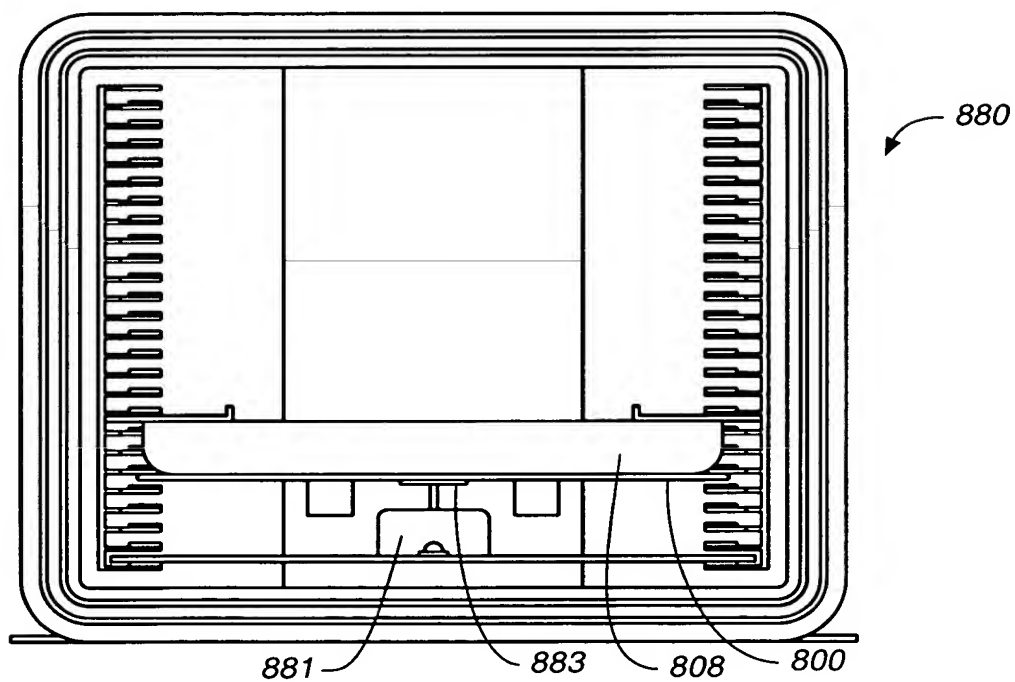
FIG._8C

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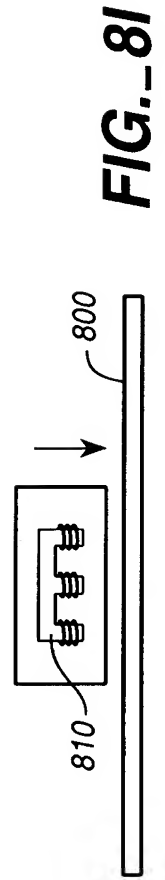
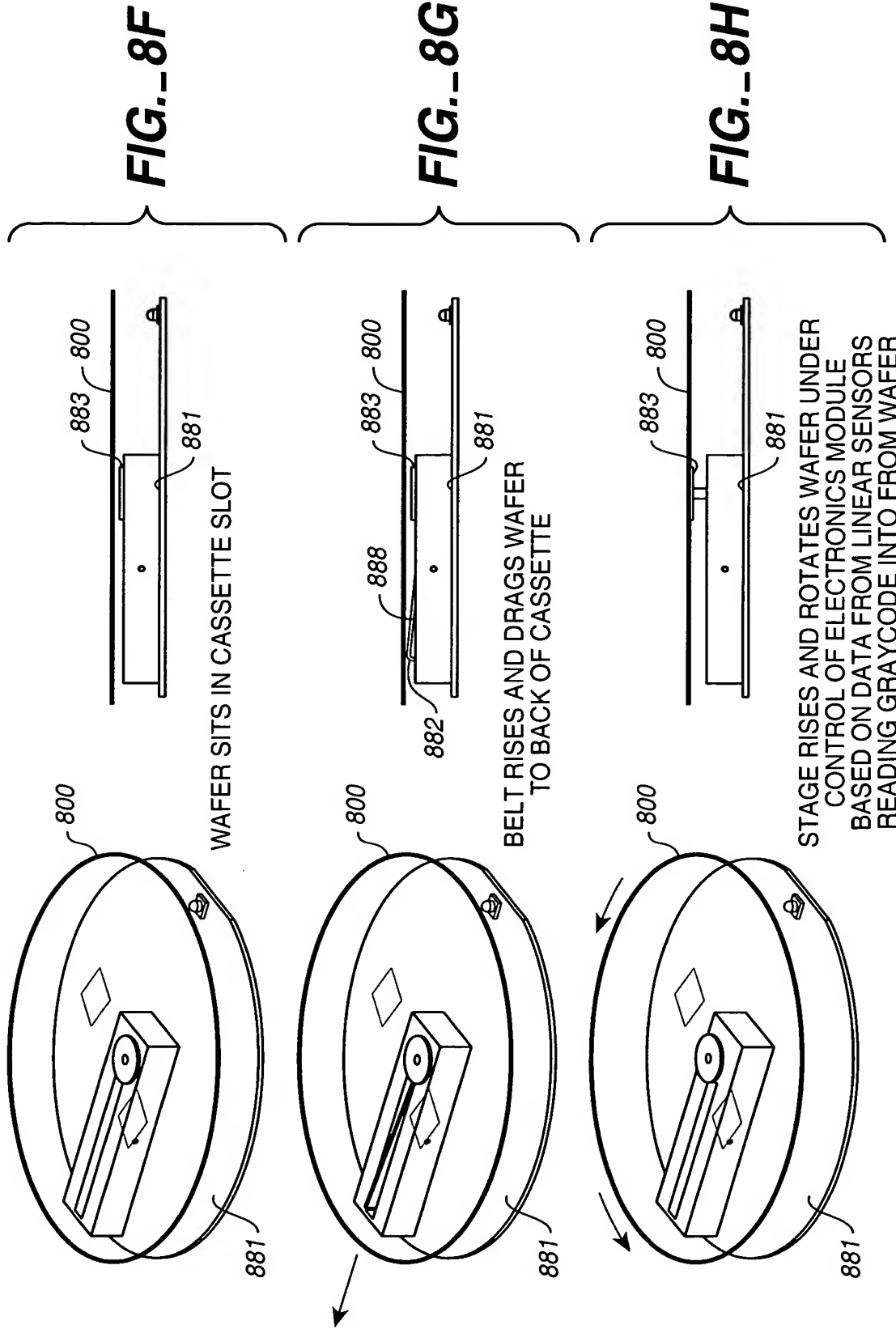
WAFER IN SLOT READY TO PICK UP

FIG._8D



WAFER RAISED FOR ROTATION ALIGNMENT AND CHARGING

FIG._8E



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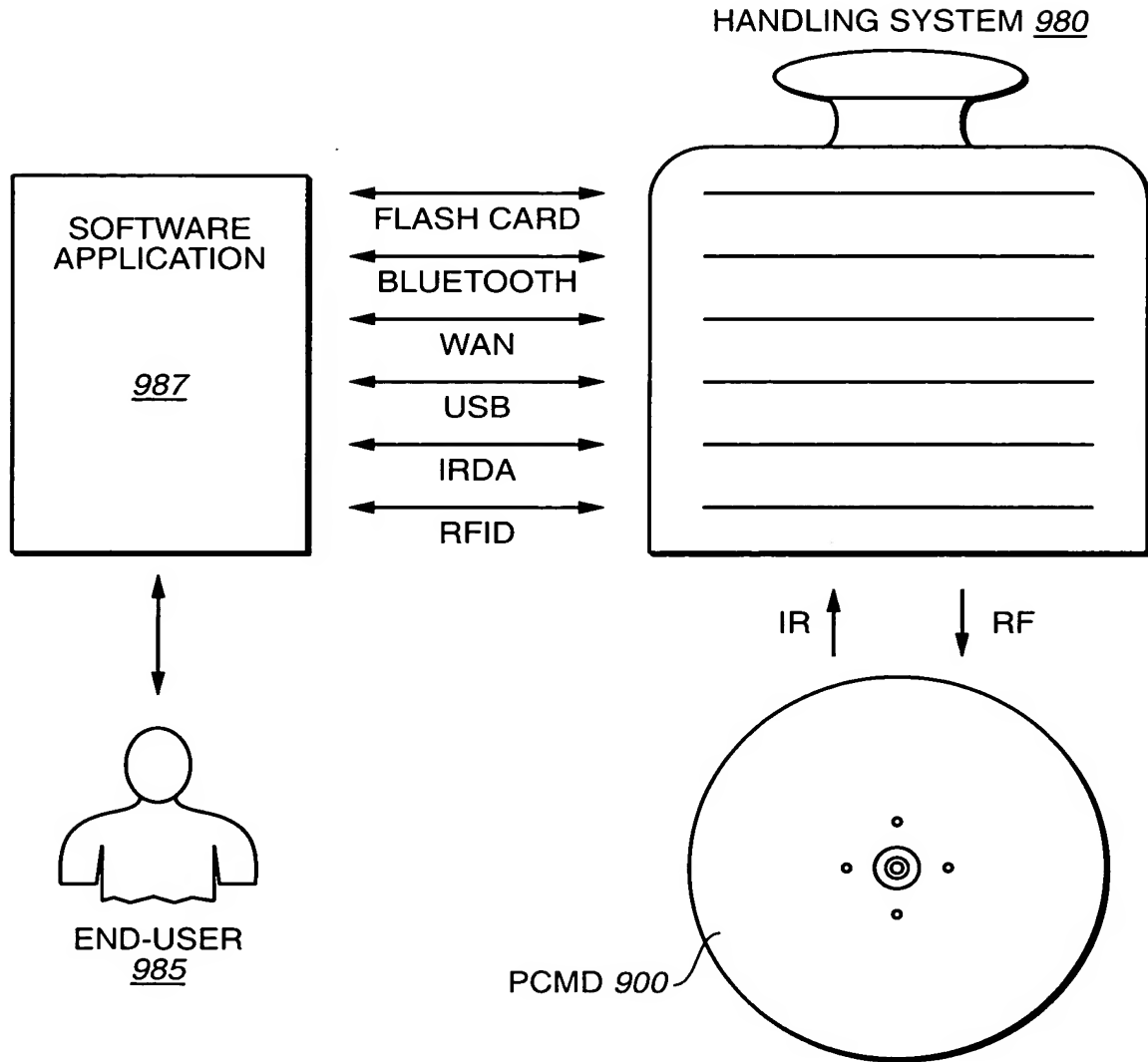


FIG._9

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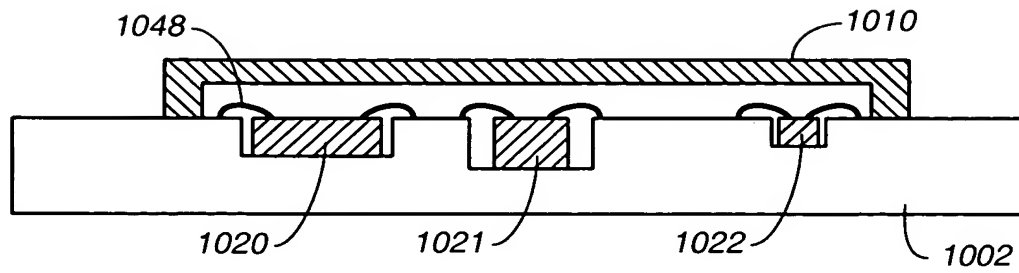


FIG._10A

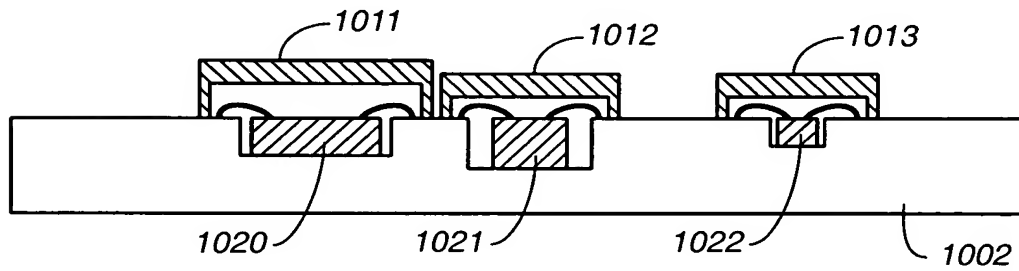


FIG._10B

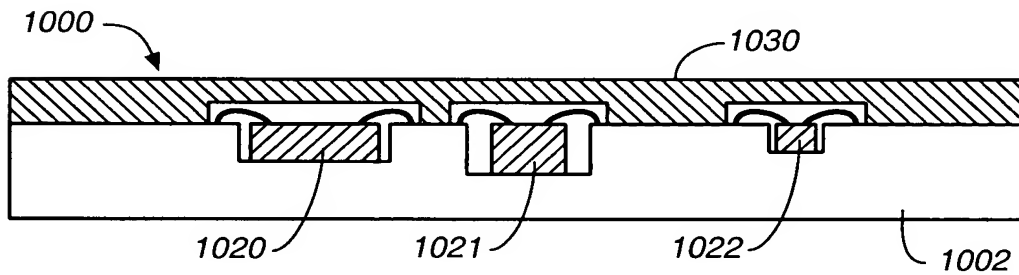


FIG._10C

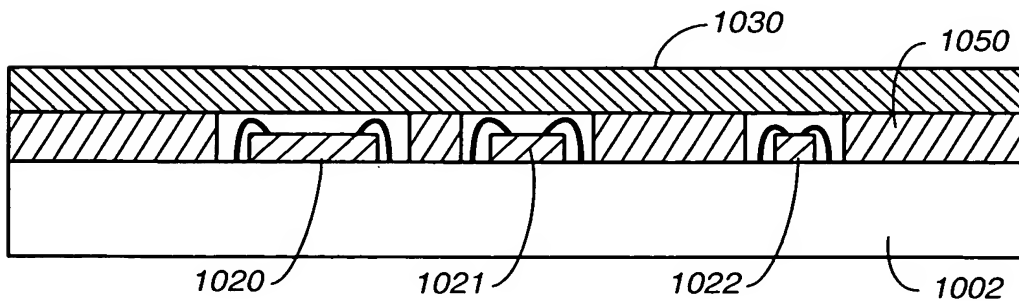


FIG._10D